## IN THE CLAIMS

Please amend the claims as follows.

1. (Currently Amended) A circuit for providing transmission rate compensation, comprising:

(a) a transmit path configured to receive downstream coefficients in a frequency domain at a first data rate and to generate a block of upstream digital samples at a second data rate; and

(b) a receive path configured i) to receive a block of downstream digital samples in a time domain at the second data rate and ii) to generate downstream coefficients in the frequency domain at a third data rate, wherein:

the first data rate is different from the second data rate; and

the transmit path comprises:

(1) a zero-padding module configured to append one or more zeros to each set of received downstream coefficients; and

(2) an inverse transform module configured to convert each set of zero-padded downstream coefficients into a corresponding block of downstream digital samples at the second data rate.

2. (Original) The invention as recited in claim 1, wherein the transmit and receive paths are coupled between a digital multi-tone (DMT) transceiver and a codec, and the blocks of upstream digital samples are generated for the codec and the blocks of downstream digital samples are generated by the codec.

3. (Original) The invention as recited in claim 1, wherein the inverse transform module in the transmit path further comprises an interpolator to generate the downstream digital samples at the second data rate.

4. (Original) The invention as recited in claim 1, wherein the transmit path further includes an intermediate inverse transform module applying an intermediate inverse transform to the received downstream coefficients to generate intermediate digital samples, an interpolator interpolating the intermediate digital samples, and an intermediate transform module applying an

intermediate transform to the upstream coefficients to generate the upstream coefficients for the inverse transform module.

5. (Original) The invention as recited in claim 1, wherein the transmit path further includes a filter reducing or eliminating signal components at frequencies generated from block boundary effects.

6. (Original) The invention as recited in claim 1, wherein the inverse transform module applies an N-point, complex fast Fourier transform (FFT) to the zero-padded downstream coefficients, and the upstream coefficients are generated with an N-point, complex FFT, N an integers greater than 1.

7. (Original) The invention as recited in claim 1, wherein the transmit path further includes a filter reducing or eliminating signal components at frequencies generated from block boundary effects.

8. (Original) The invention as recited in claim 1, wherein the transmit path further includes a copy and add module that processes the downstream digital samples to provide a periodic signal.

9 (Original) The invention as recited in claim 1, wherein the circuit is embodied in an integrated circuit.

10. (Original) The invention as recited in claim 1, wherein the circuit is implemented a modem including a digital multi-tone transceiver coupled to the transmit and receive paths.

11. (Currently Amended) In a signal processing application, a method of providing transmission rate compensation for a circuit having a receive path configured i) to receive a block of downstream digital samples in a time domain at a first data rate and ii) to generate downstream coefficients in a frequency domain, the method comprising the steps of:

(a) receiving upstream coefficients representing a signal in the frequency domain at a second data rate in a transmit path, wherein the first data rate is greater than the second data rate;

(b) appending one or more zeros to each set of upstream coefficients in the transmit path; and

(c) applying an inverse transform to convert each set of zero-padded upstream coefficients into a corresponding block of upstream digital samples representing the signal and at a compensated transmission rate in proportion to the first data rate.

12. (Original) The invention as recited in claim 11, wherein, for step (a), the transmit and receive paths are coupled between a digital multi-tone (DMT) transceiver and a codec, and step (c) further comprises the step of providing the block of upstream digital samples to the codec.

13. (Original) The invention as recited in claim 11, wherein step (c) comprises the step (c1) of interpolating a sequence of samples generated by applying the inverse transform to each set of zero-padded upstream coefficients to generate the downstream digital samples at the second data rate.

14. (Original) The invention as recited in claim 11, wherein step (a) further comprises the steps of:

(a1) applying an intermediate inverse transform to the received downstream coefficients to generate intermediate digital samples;

(a2) interpolating the intermediate digital samples; and applying an intermediate transform to the intermediate digital samples to generate the upstream coefficients.

15. (Original) The invention as recited in claim 11, wherein the transmit path further includes a filter reducing or eliminating signal components at frequencies generated from block boundary effects.

16. (Original) The invention as recited in claim 11, wherein step (c) applies an N-point, complex fast Fourier transform (FFT) to the zero-padded downstream coefficients, and the upstream coefficients are generated with an N-point, complex FFT, N an integers greater than 1.

17. (Original) The invention as recited in claim 11, further comprising the step of filtering the signal represented by the downstream digital samples to reducing or eliminating signal components at frequencies generated from block boundary effects.

18. (Original) The invention as recited in claim 11, further comprising the step of processing the downstream digital samples to provide a periodic signal.

19. (Original) The invention as recited in claim 11, wherein the method is implemented by at least one processor embodied in an integrated circuit.

20. (Original) The invention as recited in claim 11, wherein the method is implemented in a processor of a modem including a digital multi-tone transceiver as the transceiver.

21. (Currently Amended) A computer-readable medium having stored thereon a plurality of instructions, the plurality of instructions including instructions which, when executed by a processor, cause the processor to implement a method for providing transmission rate compensation for a circuit having a receive path configured i) to receive a block of downstream digital samples in a time domain at a first data rate and ii) to generate downstream coefficients in a frequency domain, the method comprising the steps of:

(a) receiving upstream coefficients representing a signal in the frequency domain at a second data rate in a transmit path, wherein the first data rate is greater than the second data rate;

(b) appending one or more zeros to each set of upstream coefficients in the transmit path; and

(c) applying an inverse transform to convert each set of zero-padded upstream coefficients into a corresponding block of upstream digital samples representing the signal and at a compensated transmission rate in proportion to the first data rate.